# Synopsys Design Constraints Sdc Basics VIsi Concepts

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functional and behavioral verification of correctness forms the bottleneck in current vlsi design systems for economical reasons design of vlsi circuits must be completely validated before manufacturing current vlsi validation is mainly done through extensive simulation the emerging alternative is based on formal design and verification methods that guarantee correctness this book describes original work in all aspects of formal hardware design methods topics covered include high level specification hardware description languages formal hardware verification methods guided synthesis methods correctness preserving transformations use of theorem provers for verification formal proof of correctness mos timing verification methods design for verifiability and practical experiences

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